1. A method for making random access memory (RAM) capacitors in a shallow trench isolation comprising the steps of:

providing a substrate having said shallow trench isolation surrounding active device areas;

forming a pad oxide layer on said substrate;

forming a first hard-mask layer on said pad oxide layer;

forming a photoresist mask having openings that lie over and within said shallow trench isolation areas;

anisotropically etching recesses in said first hard-mask layer, said pad oxide layer, and partially into said shallow trench isolation and leaving portions of said shallow trench isolation along edges of said active device areas thereby preventing plasma-etching damage to said active device areas during said etching;

isotropically etching exposed surfaces of said shallow trench isolation and removing said portions and recessing said pad oxide layer under said first hard-mask layer to expose said substrate for capacitor node contacts;

depositing a conformal first conducting layer and etching back to said first hard-mask layer to form capacitor bottom electrodes in said recesses;

forming an interelectrode dielectric layer over

said bottom electrodes; and

depositing a conformal second conducting layer to fill up said recesses.

2. The method of claim 1, further comprising:

forming a second hard-mask layer;

patterning said second hard-mask layer and said second conducting layer to form said RAM capacitors;

forming sidewall spacers on sidewalls of said RAM capacitors;

forming a gate oxide on said substrate;

depositing a third conducting layer and patterning to form gate electrodes on said substrate and over said RAM capacitors.

3. The method of claim 1, wherein said substrate is a silicon substrate.

4. The method of claim 1, wherein said pad oxide is formed on said substrate to a thickness of between about 50 and 300 Angstroms.

5. The method of claim 1, wherein said first hard-mask layer is silicon nitride and is deposited to a thickness of between about 100 and 500 Angstroms.

6. The method of claim 1, wherein said anisotropic etching is carried out in a high-density plasma etcher using an etchant gas mixture of CHF_3.

7. The method of claim 1, wherein said isotropic etching is carried out using HF/H_2O solution.

8. The method of claim 1, wherein said first conducting layer is a material selected from the group that includes polysilicon, TiN, WN, MoN, WSiN, TiW, TaN, and Ta.

9. The method of claim 1, wherein said first conducting layer is deposited to a thickness of between about 200 and 800 Angstroms.

10. The method of claim 1, wherein said first conducting layer is etched back to said first hard-mask layer using chemical-mechanical polishing.

11. The method of claim 1, wherein said inter-electrode dielectric layer is silicon oxide/silicon nitride/silicon oxide and is formed to a thickness of between about 30 and 100 Angstroms.

12. The method of claim 1, wherein said second

conducting layer is a material selected from the group that includes polysilicon, TiN, WN, MoN, WSiN, TiW, TaN, and Ta.

13. The method of claim 1, wherein said second conducting layer is deposited sufficiently thick to fill said recesses and to form a planar surface over said recesses.

14. The method of claim 2, wherein said second hard-mask layer is silicon oxynitride formed by plasma-enhanced chemical vapor deposition (PECVD) to a thickness of between about 100 and 800 Angstroms.

15. The method of claim 2, wherein said sidewall spacers are formed on said sidewalls of said RAM capacitors by depositing a conformal insulating layer and anisotropically etching back.

16. The method of claim 2, wherein said gate oxide is formed by thermal oxidation to a thickness of between about 10 and 150 Angstroms.

17. The method of claim 2, wherein said third conducting layer is a material selected from the group that includes polysilicon, TiN, WN, MoN, WSiN, TiW,

TaN, and Ta.

18. The method of claim 2, wherein said third conducting layer is deposited to a thickness of between about 500 and 3000 Angstroms.

19. A random access memory (RAM) capacitor in a shallow trench isolation comprised of:

a substrate having said shallow trench isolation surrounding active device areas;

a pad oxide layer on said substrate;

a first hard-mask layer on said pad oxide layer;

recesses in said first hard-mask layer, said pad oxide layer, and partially within said shallow trench isolation and said recesses extending under said first hard-mask layer to said substrate and said recesses having a bottle-shape;

a conformal first conducting layer in said recesses for capacitor bottom electrodes;

an interelectrode dielectric layer over said bottom electrodes;

a conformal second conducting layer that fills said recesses sufficiently thick to form a planar surface over said recesses.

20. The structure of claim 19, further comprising:

a planar second hard-mask layer over said second conducting layer and said second hard-mask layer and said second conducting layer having a pattern to form capacitor top electrodes having sidewall spacers;

a gate oxide on said substrate;

a third conducting layer patterned for gate electrodes on said substrate and over said RAM capacitors.

21. The structure of claim 19, wherein said substrate is a silicon substrate.

22. The structure of claim 19, wherein said pad oxide is silicon oxide and has a thickness of between about 50 and 300 Angstroms.

23. The structure of claim 19, wherein said first hard-mask layer is silicon nitride and has a thickness of between about 100 and 500 Angstroms.

24. The structure of claim 19, wherein said first conducting layer is a material selected from the group that includes polysilicon, TiN, WN, MoN, WSiN, TiW, TaN, and Ta.

25. The structure f claim 19, wherein said first

conducting layer has a thickness of between about 100 and 500 Angstroms.

26. The structure of claim 19, wherein said inter-electrode dielectric layer is silicon oxide/silicon nitride/silicon oxide and has a thickness of between about 30 and 100 Angstroms.

27. The structure of claim 19, wherein said second conducting layer is a material selected from the group that includes polysilicon, TiN, WN, MoN, WSiN, TiW, TaN, and Ta.

28. The structure of claim 20, wherein said second hard-mask layer is silicon oxynitride and has a thickness of between about 100 and 800 Angstroms.

29. The structure of claim 20, wherein said sidewall spacers are an insulating material.

30. The structure of claim 20, wherein said gate oxide is a thermal oxide and has a thickness of between about 10 and 150 Angstroms.

31. The structure of claim 20, wherein said third conducting layer is a material selected from the group

that includes polysilicon, TiN, WN, MoN, WSiN, TiW, TaN, and Ta.

32. The structure of claim 20, wherein said third conducting layer has a thickness of between about 500 and 3000 Angstroms.